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10/552,816	10/11/2005	Raf Lodewijk Jan Roovers	NL 030433	5559

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EXAMINER	
SHAH, TANMAY K	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
02/13/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/552,816	ROOVERS ET AL.	
	Examiner	Art Unit	
	TANMAY K. SHAH	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Amendment filed on 11/07/08.

Response to Arguments

2. Applicant's arguments filed on 11/07/08 have been fully considered but they are not persuasive.

Applicant is reminded that a rejection is made en light of the entire reference cited by examiner.

Regarding claim 1, applicant argues that applied reference does not teach or disclose a sampling time generator, for generating signals indicative of a plurality of sampling time points.

In response to above-mentioned arguments, applicant's interpretation of the applied reference has been considered. However, the applied reference teaches limitations of argued matter.

As shown in Fig. 5 it comprises plurality of comparators coupled to receive a charge pump feedback bias signal for comparison to a plurality of threshold voltage levels. the charge pump feedback bias signal may be sampled as shown in Fig. 4 or in an alternate method according to design preference. so it can be sampled and then compared it to plurality of the voltage level from comparators. As disclosed in Anand, as it will be sampled, it will have more than one sampling points so it is considered as plurality of sampling time points (**page 11, line 25 - 35**).

Also, applicant argues that it does not disclose wherein each of the comparators is programmable with a sampling time point selected from said plurality of sampling time points and with a reference level selected form said plurality of reference levels.

In response to above-mentioned arguments, applicant's interpretation of the applied reference has been considered. However, the applied reference teaches limitations of argued matter.

As described in Anand that the plurality of comparators is connected to the finite state machine. the finite state machine and comparators are considered as a whole comparators. also, Finite state machine 504 further is coupled to receive control signals from an external source. Finite state machine 504 comprises logic circuitry formed using any one of a plurality of designs and technologies, including ASIC designs, field programmable gate array design (FPGA) and general purpose processor technology whose operational logic is defined by software. In general, however, finite state machine 504 is formed to define operational logic that is disclosed herein in the description of its operation (**i.e. page 11, col 46 - 54**). So it can be programmed depending on the desired output. also, sampling time point selected from said plurality of sampling time points and with a reference level selected from said plurality of reference levels.

Applicant also argues that Anand does not teach or disclose both the generated signals indicative of a plurality of sampling points and a received signal applied to each of the comparators.

In response to above-mentioned arguments, applicant's interpretation of the applied reference has been considered. However, the applied reference teaches limitations of argued matter.

Anand teaches In the described embodiment of the invention, four comparators 512, 516, 520 and 524 each receive the charge pump feedback bias signal 508 at a positive terminal for comparison to one of four specified voltage levels that are received at a negative terminal. More specifically, comparator 512 further is coupled to receive at its negative terminal, a high threshold voltage level, while comparator 516 receives a low threshold voltage level at its negative terminal. Comparators 520 and 524 receive high and low error threshold voltage level, respectively. The outputs of comparators 512, 516, 520 and 524 are produced to a finite state machine 504. Finite state machine 504 further is coupled to receive control signals from an external source (col 11, line 34 - 45). The finite state machine and comparators are considered as a whole comparators So it teaches receiving signals to comparator and then receiving reference voltage level signal.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1- 12 are rejected under 35 U.S.C. 102(b) as being anticipated by **Anand (US 2003/0224747)**.

Regarding claim 1, **Anand** teaches a communication receiver, comprising a pulse detection unit, for detecting pulses in a received signal, the pulse detection unit comprising:

a plurality of comparators (**i.e. plurality of comparators, 512,516,520,524 of Fig. 5, page 6, paragraph 58**);

a sampling time generator, for generating signals indicative of a plurality of sampling time points (**i.e. the charge pump feedback bias signal may be sampled as shown in Fig. 4, page 6, paragraph 58**); and

a reference level generator, for generating a plurality of reference levels (**i.e. plurality of threshold voltage levels, page 6, paragraph 58**),

wherein each of the comparators is programmable with a sampling time point selected from said plurality of sampling time points and with a reference level selected from said plurality of reference levels (**i.e. finite state machine is comprising logic circuitry formed using any one of a plurality of designs and technologies, including ASIC design, Field programmable gate array (FPGA) and general purpose processor technology whose operation logic is defined by software, page 6, paragraph 58**), and

wherein the received signal is applied to each of the comparators such that each of the comparators produces a respective output signal based on a comparison between the received signal level and the selected reference level at

the selected sampling time point **(i.e. four comparators each receive the charge pump feedback bias signal at a positive terminal for comparison to one of four specified voltage levels that are received at a negative terminal. The output of comparators are produced to a finite state machine, page 6, paragraph 58, also, four comparators 512, 516, 520 and 524 each receive the charge pump feedback bias signal 508 at a positive terminal for comparison to one of four specified voltage levels that are received at a negative terminal. More specifically, comparator 512 further is coupled to receive at its negative terminal, a high threshold voltage level, while comparator 516 receives a low threshold voltage level at its negative terminal. Comparators 520 and 524 receive high and low error threshold voltage level, respectively. The outputs of comparators 512, 516, 520 and 524 are produced to a finite state machine 504. Finite state machine 504 further is coupled to receive control signals from an external source (col 11, line 34 - 45).**).

Regarding claim 2, **Anand teaches** communications receiver as claimed in claim 1, comprising a signal processor, for detecting pulses in the received signal based on the output signals from the comparators **(i.e. The output of comparators are produced to a finite state machine ,finite state machine is comprising logic circuitry formed using any one of a plurality of designs and technologies, including ASIC design, Field programmable gate array**

(FPGA) and general purpose processor technology whose operation logic is defined by software, page 6, paragraph 58).

Regarding claim 3, **Anand teaches** communications receiver as claimed in claim 2, wherein the signal processor is adapted to program the comparators with respective selected sampling time points and reference levels, in order to detect said pulses (**i.e. The output of comparators are produced to a finite state machine ,finite state machine is comprising logic circuitry formed using any one of a plurality of designs and technologies, including ASIC design, Field programmable gate array (FPGA) and general purpose processor technology whose operation logic is defined by software, page 6, paragraph 58**).

Regarding claim 4, **Anand teaches** a communications receiver as claimed in claim 1, comprising a pre-amplifier, for pre-amplifying the received signal to an appropriate level for comparison with the plurality of reference levels (**i.e. an RF receiver unit includes a receiver/ low noise amplifier (LNA) that is coupled to receiver wireless radio communications by the way of an antenna, page , paragraph 45**).

Regarding claim 5, **Anand teaches** a communications receiver as claimed in claim 1, wherein the reference level generator is adapted to scale the generated plurality of reference levels for comparison with the received signal (**i.e. four comparators each receive the charge pump feedback bias signal at a positive terminal for comparison to one of four specified voltage levels that are received at a negative terminal. Page 6, paragraph 58**).

Regarding claim 6, **Anand teaches** a communications receiver as claimed in claim 1, further comprising a current reference, for driving bias currents to said plurality of comparators (**i.e. each receive the charge pump feedback bias signal at a positive terminal for comparison, page 6, paragraph 58**).

Regarding claim 7, a method has substantially same limitations as claim 1, thus the same rejection is applicable.

Regarding claim 8, a method has substantially same limitations as claim 2, thus the same rejection is applicable

Regarding claim 9, a method has substantially same limitations as claim 4, thus the same rejection is applicable.

Regarding claim 10, a method has substantially same limitations as claim 5, thus the same rejection is applicable.

Regarding claim 11, **Anand teaches** a method as claimed in claim 7, comprising programming the comparators with respective selected sampling time points and reference levels, based on knowledge about the possible shapes of said pulses (**i.e. more specifically, comparator further is coupled to receive at its negative terminal, h high threshold level, while comparator receives a low threshold voltage level, page 6, paragraph 58**).

Regarding claim 12, **Anand teaches** a method as claimed in claim 7, comprising programming the comparators with respective selected sampling time points and reference levels (**i.e. The output of comparators are produced to a finite state machine ,finite state machine is comprising logic circuitry formed using any one of a plurality of designs and technologies, including ASIC design, Field programmable gate array (FPGA) and general purpose processor technology whose operation logic is defined by software, page**

6, paragraph 58), based on knowledge about the expected arrival times of said pulses (**i.e. signal which is set according to whether sufficient time has elapsed since last calibration step, page 6, paragraph 59**).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TANMAY K. SHAH whose telephone number is (571)270-3624. The examiner can normally be reached on Mon-Thu (7:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. K. S./
Examiner, Art Unit 2611

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611